Lenovo

ThinkSystem SN850 Compute Node Memory Population Reference

Machine Types: 7X15

Note

Before using this information and the product it supports, be sure to read and understand the safety information and the safety instructions, which are available at:
https://pubs.lenovo.com/safety_documentation/pdf_files.html

In addition, be sure that you are familiar with the terms and conditions of the Lenovo warranty for your server, which can be found at:
http://datacentersupport.lenovo.com/warrantylookup

Fifth Edition (December 2022)

Contents

Chapter 1. Memory guidelines

There are a number of criteria that must be followed when installing memory modules in your compute node.

Populating memory modules for best system performance

The DIMM (memory) population sequences in this document show all memory population combinations that are supported by your compute node. Some of these combinations will perform better than others because they balance the distribution of memory across processors, memory controllers, and memory channels. Balanced memory configurations enable optimal interleaving across all populated memory channels of a processor to boost memory performance. To populate balanced memory configurations for the best memory performance, observe the following guidelines:

- When multiple processors are installed, balance the DIMMs across the processors so all processors have the same memory capacity.
- Balance the DIMMs across the processor memory controllers so all memory controllers have exactly the same memory DIMM population and memory capacity. Each processor in your compute node has two memory controllers, each memory controller has three memory channels, and each memory channel has two DIMM slots.
- Populate all memory channels for optimal performance.
- For each memory controller, balance the DIMMs across all memory channels so all memory channels are configured with the same number of DIMMs, the same total memory capacity, and the same total number of memory ranks.
- For memory configurations that do not require or allow use of all memory channels, all memory channels that are populated should have the same number of DIMMs, the same total memory capacity, and the same total number of memory ranks.

Where supported by specific memory population configurations, performance can be further enhanced by following these guidelines:

- Select DIMMs by ranks for each populated memory channel, so the total number of ranks on each channel is an even number.
- Select identical DIMMs to populate the DIMM slots for each populated memory channel when populating more than one DIMM slot per memory channel. For example, configure two identical 16 GB DIMMs on each populated memory channel. It is not required that the DIMMs on each memory channel be identical for the compute node to function, but memory performance will be slightly improved when using identical DIMMs.

Other rules when installing memory

When installing memory modules, observe the following criteria:

- Install memory modules following only the sequences shown in Chapter 2 “Memory module installation order” on page 3.
- Do not mix RDIMMs and LR-DIMMs in the same compute node.
- Install higher capacity (ranked) DIMMs first, following the specified population sequence.
- Installing or removing DIMMs changes the compute node configuration. When you restart the compute node, it displays a message that indicates that the memory configuration has changed. To view the compute node configuration, use the Setup utility.

Chapter 2. Memory module installation order

Memory modules must be installed in a specific order based on the memory configuration that you implement and the number of processors and memory modules installed in the compute node.

Note: List of supported memory module is different for 1st generation (Skylake) and 2nd generation (Cascade Lake) Intel Xeon processors. Make sure to install compatible memory modules to avoid system error. For a list of supported DIMMs, see: https://serverproven.lenovo.com/.

The following memory configurations and population sequences are supported for the ThinkSystem SN850:

Memory installation requirements:

- A label on each DIMM identifies the DIMM type. This information is in the format **xxxxx *n*Rxxx PC4-xxxxx-xx-xx-xxx**. Where ***n*** indicates if the DIMM is single-rank (n=1) or dual-rank (n=2).
- At least one DIMM is required or each processor. Install at least six DIMMs per processor for good performance.
- The following table includes all the feasible combinations of different types of DIMMs:

Table 1. DIMM compatibility

DIMM Types	RDIMM	LRDIMM	3DS RDIMM
RDIMM	V	X	X
LRDIMM	X	V	X
3DS RDIMM	X	X	V

- When you replace a DIMM, the compute node provides automatic DIMM enablement capability without requiring you to use the Setup utility to enable the new DIMM manually.

Attention:

- Mixing x4 and x8 DIMMs in the same channel is allowed.
- Install DIMMs of the same speed for optimal performance. Otherwise, the BIOS will find and run the lowest speed among all channels.
- Always populate DIMMs with the maximum number of ranks in the farthest DIMM slot, followed by the nearest DIMM slot.

Independent memory mode

In independent memory mode, memory channels can be populated with DIMMs in any order and you can populate all channels for each processor in any order with no matching requirements. Independent memory mode provides the highest level of memory performance, but lacks failover protection. The DIMM installation order for independent memory mode varies based on the number of processors and memory modules installed in the compute node.

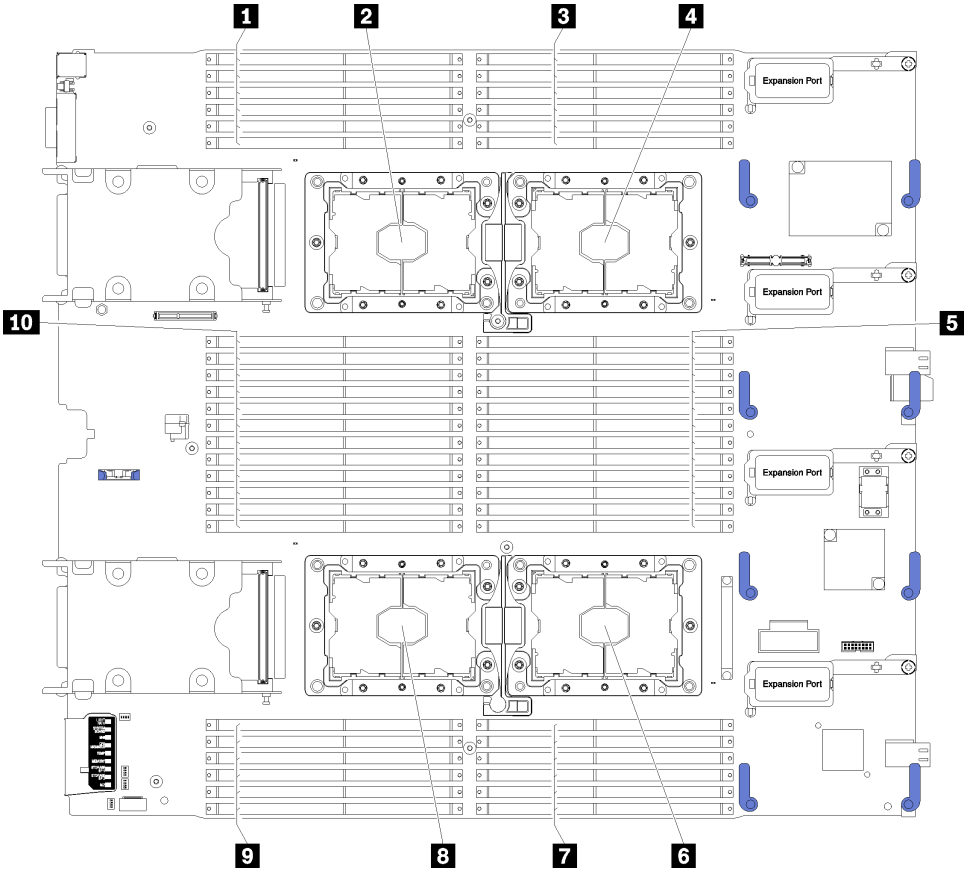

Figure 1. Processor and memory module layout

Table 2. Processor and memory module layout

1 DIMM 25 – 30	6 Processor socket 2
2 Processor socket 3	7 DIMM 19 – 24
3 DIMM 1 – 6	8 Processor socket 4
4 Processor socket 1	9 DIMM 43 – 48
5 DIMM 7 – 18	10 DIMM 31 – 42

Table 3. Channel and slot information of DIMMs around processor 1 and 2

Memory controllers	Controller 0						Controller 1					
Channels	Channel 2		Channel 1		Channel 0		Channel 0		Channel 1		Channel 2	
Slots	0	1	0	1	0	1	1	0	1	0	1	0
DIMM numbers (processor 1)	1	2	3	4	5	6	7	8	9	10	11	12
DIMM numbers (processor 2)	13	14	15	16	17	18	19	20	21	22	23	24

Table 4. Channel and slot information of DIMMs around processor 3 and 4

Memory controllers	Controller 1						Controller 0					
Channels	Channel 2		Channel 1		Channel 0		Channel 0		Channel 1		Channel 2	
Slots	0	1	0	1	0	1	1	0	1	0	1	0
DIMM numbers (processor 3)	25	26	27	28	29	30	31	32	33	34	35	36
DIMM numbers (processor 4)	37	38	39	40	41	42	43	44	45	46	47	48

Independent memory mode guidelines:

- Individual memory channels can run at different DIMM timings, but all channels must run at the same interface frequency.
- Populate memory channel 0 first.
- Memory channel 1 is empty or identically populated as memory channel 0.
- Memory channel 2 is empty or identically populated as memory channel 1.
- In each memory channel, populate slot 0 first.
- If a memory channel has two DIMMs, populate the DIMM with a higher number of ranks in slot 0. If the ranks are the same, populate the one with higher capacity in slot 0.

Notes: Two special rules of identical DIMMs population for optimal performance.

- When a processor populates three identical DIMMs (same part number), populate all on memory controller 0; otherwise, follow the general population rule.
- When a processor populates ten identical DIMMs (same part number), populate;five DIMMs on memory controller 0 and five DIMMs on memory controller 1; otherwise, follow the general population rule.

The independent memory mode DIMM population sequences for each supported processor configuration are:

- “Installation order: independent memory mode with two processors” on page 6
- “Installation order: independent memory mode with four processors” on page 7

Installation order: independent memory mode with two processors

Memory module installation order for independent (non-mirroring) memory mode with two processors installed in the compute node.

The following table shows the DIMM population sequence for independent memory mode when two processors are installed.

Note: When adding one or more DIMMs during a memory upgrade, you might need to move other DIMMs that are already installed to new locations.

Table 5. Independent mode with two processors

Total	Processor 1												Processor 2												Total
DIMMs	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	DIMMs
2					5												17								**2**
4					5			8									17			20					**4**
6			3		5			8							15		17			20					**6**
8			3		5			8		10					15		17			20		22			**8**
10	1		3		5			8		10			13		15		17			20		22			**10**
12	1		3		5			8		10		12	13		15		17			20		22		24	**12**
14			3	4	5	6		8		10		12			15	16	17	18		20		22		24	**14**
16			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**16**
18	1	2	3	4	5	6		8		10		12	13	14	15	16	17	18		20		22		24	**18**
20	1	2	3	4	5	6	7	8	9	10			13	14	15	16	17	18	19	20	21	22			**20**
22	1	2	3	4	5	6	7	8	9	10		12	13	14	15	16	17	18	19	20	21	22		24	**22**
24	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**24**

Installation order: independent memory mode with four processors

Memory module installation order for independent (non-mirroring) memory mode with four processors installed in the compute node.

The following tables show the DIMM population sequence for independent memory mode when four processors are installed.

Note: When adding one or more DIMMs during a memory upgrade, you might need to move other DIMMs that are already installed to new locations.

Table 6. Independent mode with four processors (Processors 1 and 2, 4 to 48 total DIMMs installed in compute node)

Total	Processor 1												Processor 2												Total
DIMMs	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	DIMMs
4					5												17								**4**
8					5			8									17			20					**8**
12			3		5			8							15		17			20					**12**
16			3		5			8		10					15		17			20		22			**16**
20	1		3		5			8		10			13		15		17			20		22			**20**
24	1		3		5			8		10		12	13		15		17			20		22		24	**24**
28			3	4	5	6		8		10		12			15	16	17	18		20		22		24	**28**
32			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**32**
36	1	2	3	4	5	6		8		10		12	13	14	15	16	17	18		20		22		24	**36**
40	1	2	3	4	5	6	7	8	9	10			13	14	15	16	17	18	19	20	21	22			**40**
44	1	2	3	4	5	6	7	8	9	10		12	13	14	15	16	17	18	19	20	21	22		24	**44**
48	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**48**

Related DIMM population sequences for four processor systems:

To continue populating processor 3 and 4 DIMMs for a system with 4 to 48 DIMMs, see Table 7 “Independent mode with four processors (Processors 3 and 4, 4 to 48 total DIMMs installed in compute node)” on page 8.

Table 7. Independent mode with four processors (Processors 3 and 4, 4 to 48 total DIMMs installed in compute node)

Total	Processor 3												Processor 4												Total
DIMMs	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	DIMMs
4								32												44					**4**
8					29			32									41			44					**8**
12					29			32		34							41			44		46			**12**
16			27		29			32		34					39		41			44		46			**16**
20			27		29			32		34		36			39		41			44		46		48	**20**
24	25		27		29			32		34		36	37		39		41			44		46		48	**24**
28	25		27		29		31	32	33	34			37		39		41		43	44	45	46			**28**
32			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			**32**
36	25		27		29		31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	**36**
40			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	**40**
44	25		27	28	29	30	31	32	33	34	35	36	37		39	40	41	42	43	44	45	46	47	48	**44**
48	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	**48**

Related DIMM population sequences for four processor systems:

To continue populating processor 1 and 2 DIMMs for a system with 4 to 48 DIMMs, see Table 6 “Independent mode with four processors (Processors 1 and 2, 4 to 48 total DIMMs installed in compute node)” on page 7.

Memory mirroring

Memory-mirroring mode provides full memory redundancy while reducing the total system memory capacity in half. Memory channels are grouped in pairs with each channel receiving the same data. If a failure occurs, the memory controller switches from the DIMMs on the primary channel to the DIMMs on the backup channel. The DIMM installation order for memory mirroring varies based on the number of processors and DIMMs installed in the compute node.

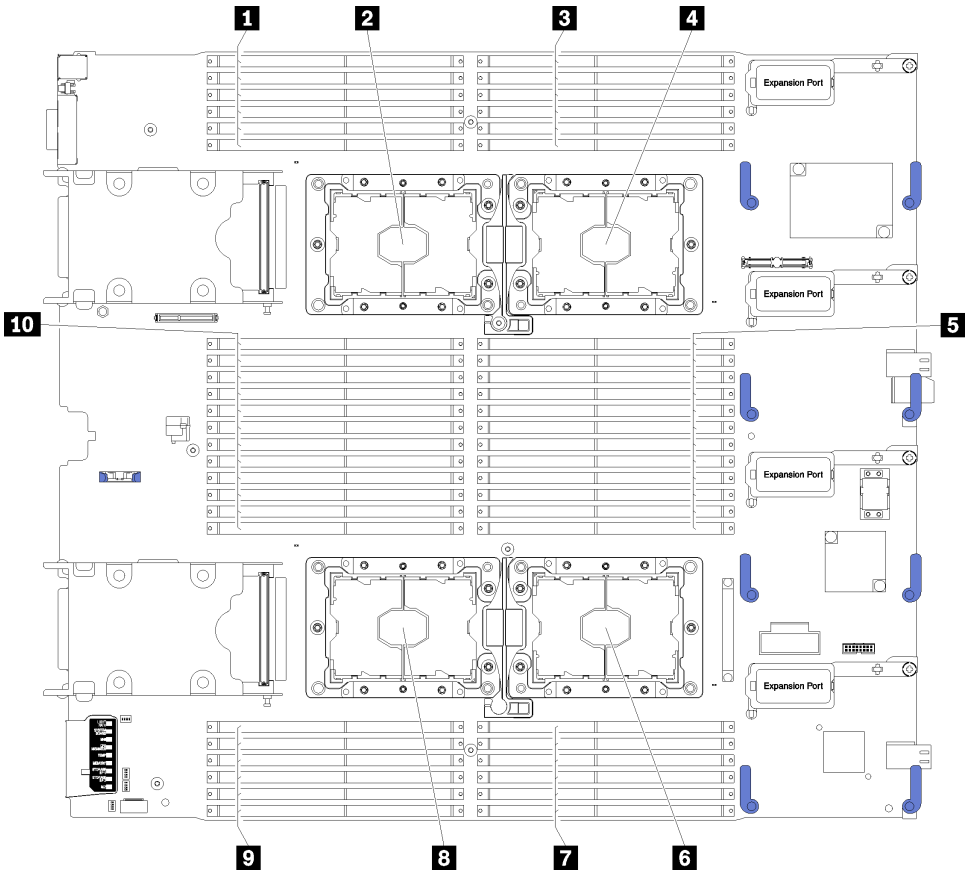

Figure 2. Processor and memory module layout

Table 8. Processor and memory module layout

1 DIMM 25 – 30	6 Processor socket 2
2 Processor socket 3	7 DIMM 19 – 24
3 DIMM 1 – 6	8 Processor socket 4
4 Processor socket 1	9 DIMM 43 – 48
5 DIMM 7 – 18	10 DIMM 31 – 42

Table 9. Channel and slot information of DIMMs around processor 1 and 2

Memory controllers	Controller 0						Controller 1					
Channels	Channel 2		Channel 1		Channel 0		Channel 0		Channel 1		Channel 2	
Slots	0	1	0	1	0	1	1	0	1	0	1	0
DIMM numbers (processor 1)	1	2	3	4	5	6	7	8	9	10	11	12
DIMM numbers (processor 2)	13	14	15	16	17	18	19	20	21	22	23	24

Table 10. Channel and slot information of DIMMs around processor 3 and 4

Memory controllers	Controller 1						Controller 0					
Channels	Channel 2		Channel 1		Channel 0		Channel 0		Channel 1		Channel 2	
Slots	0	1	0	1	0	1	1	0	1	0	1	0
DIMM numbers (processor 3)	25	26	27	28	29	30	31	32	33	34	35	36
DIMM numbers (processor 4)	37	38	39	40	41	42	43	44	45	46	47	48

Memory mirroring guidelines:

- Memory mirroring reduces the maximum available memory by half of the installed memory. For example, if the compute node has 64 GB of installed memory, only 32 GB of addressable memory is available when memory mirroring is enabled.
- DIMMS are installed in pairs for each processor. Each DIMM in a pair must be identical in size and architecture.
- DIMMs on each memory channel must be of equal density.
- If two memory channels have DIMMs, mirroring occurs across two DIMMs (channels 0/1 will both contain the primary/secondary memory caches).
- If three memory channels have DIMMs, mirroring occurs across all three DIMMs (channels 0/1, channels 1/2, and channels 2/0 will all contain primary/secondary memory caches).

Memory mirroring DIMM population sequences for each of the supported processor configurations is shown by one of the following topics:

- “Installation order: memory mirroring with two processors” on page 11
- “Installation order: memory mirroring with four processors” on page 12

Installation order: memory mirroring with two processors

Memory module installation order for memory mirroring with two processors installed in the compute node.

The following table shows the DIMM population sequence for memory mirroring when two processors are installed.

Note: When adding one or more DIMMs during a memory upgrade, you might need to move other DIMMs that are already installed to new locations.

Table 11. Memory mirroring with two processors

Total	Processor 1												Processor 2												Total
DIMMs	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	DIMMs
4			3		5										15		17								**4**
6	1		3		5								13		15		17								**6**
8			3		5			8		10					15		17			20		22			**8**
12	1		3		5			8		10		12	13		15		17			20		22		24	**12**
16			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**16**
24	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**24**

Installation order: memory mirroring with four processors

Memory module installation order for memory mirroring with four processors installed in the compute node.

The following tables show the DIMM population sequence for memory mirroring when four processors are installed.

Note: When adding one or more DIMMs during a memory upgrade, you might need to move other DIMMs that are already installed to new locations.

Table 12. Memory mirroring with four processors (Processors 1 and 2, 8 to 48 total DIMMs installed in compute node)

Total	Processor 1												Processor 2												Total
DIMMs	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	DIMMs
8			3		5										15		17								**8**
16			3		5			8		10					15		17			20		22			**16**
24	1		3		5			8		10		12	13		15		17			20		22		24	**24**
32			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**32**
48	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**48**

Related DIMM population sequences for four processor systems:

- To continue populating processor 3 and 4 DIMMs for a system with 8 to 48 DIMMs, see Table 13 “Memory mirroring with four processors (Processors 3 and 4, 8 to 48 total DIMMs installed in compute node)” on page 13.

Table 13. Memory mirroring with four processors (Processors 3 and 4, 8 to 48 total DIMMs installed in compute node)

Total	Processor 3												Processor 4												Total
DIMMs	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	DIMMs
8								32		34										44		46			**8**
16			27		29			32		34					39		41			44		46			**16**
24	25		27		29			32		34		36	37		39		41			44		46		48	**24**
32			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			**32**
48	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	**48**

Related DIMM population sequences for four processor systems:

- Processor 1 and 2 DIMM population sequences for 8 to 48 total DIMMs installed in compute node, see Table 12 “Memory mirroring with four processors (Processors 1 and 2, 8 to 48 total DIMMs installed in compute node)” on page 12.

Memory sparing

In memory-sparing mode, one memory rank serves as a spare for other ranks on the same channel in case they fail. The spare rank is held in reserve and not used as active memory until a failure is indicated, with reserved capacity subtracted from the total available memory in the system. The DIMM installation order for memory sparing varies based on the number of processors and memory modules installed in the compute node.

After an error threshold is surpassed in a system protected by memory sparing, the content of a failing rank of DIMMs is copied to the spare rank. The failing rank is then taken offline and the spare rank placed online for use as active memory in place of the failed rank. Since the failover process involves copying of memory content, the level of memory redundancy provided by memory sparing is less than that provided by memory mirroring: memory mirroring is the preferred failure-protection choice for critical applications.

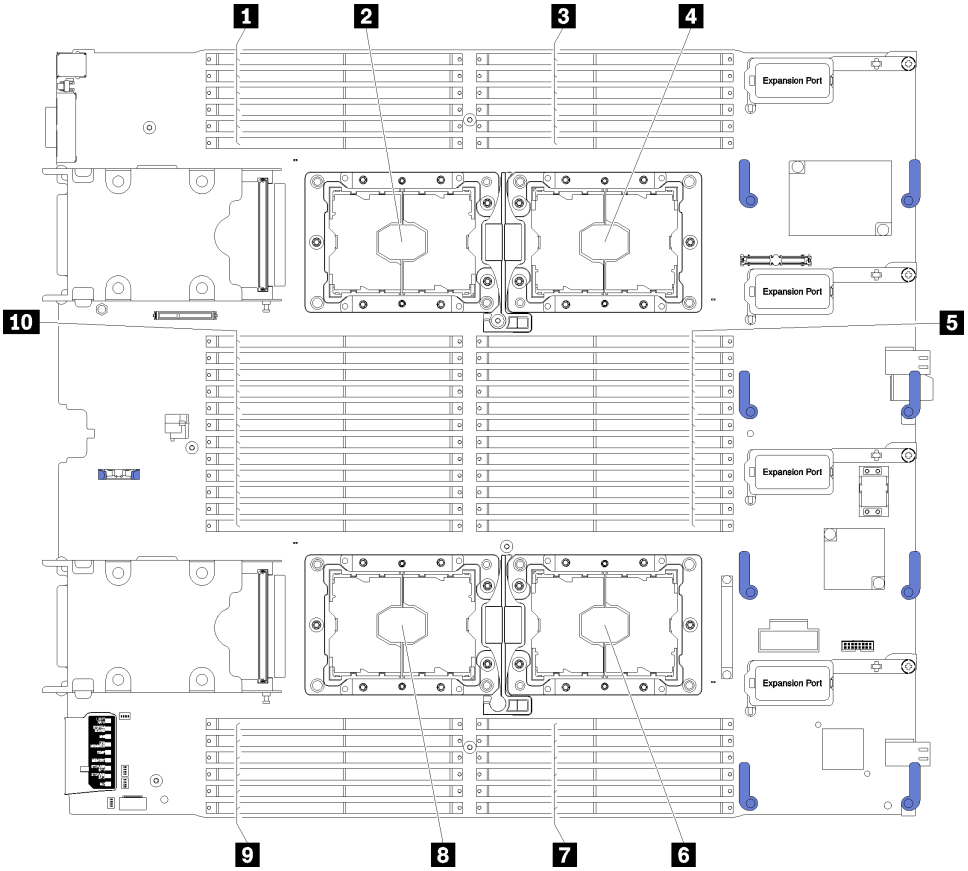

Figure 3. Processor and memory module layout

Table 14. Processor and memory module layout

1 DIMM 25 – 30	6 Processor socket 2
2 Processor socket 3	7 DIMM 19 – 24
3 DIMM 1 – 6	8 Processor socket 4
4 Processor socket 1	9 DIMM 43 – 48
5 DIMM 7 – 18	10 DIMM 31 – 42

Table 15. Channel and slot information of DIMMs around processor 1 and 2

Memory controllers	Controller 0						Controller 1					
Channels	Channel 2		Channel 1		Channel 0		Channel 0		Channel 1		Channel 2	
Slots	0	1	0	1	0	1	1	0	1	0	1	0
DIMM numbers (processor 1)	1	2	3	4	5	6	7	8	9	10	11	12
DIMM numbers (processor 2)	13	14	15	16	17	18	19	20	21	22	23	24

Table 16. Channel and slot information of DIMMs around processor 3 and 4

Memory controllers	Controller 1						Controller 0					
Channels	Channel 2		Channel 1		Channel 0		Channel 0		Channel 1		Channel 2	
Slots	0	1	0	1	0	1	1	0	1	0	1	0
DIMM numbers (processor 3)	25	26	27	28	29	30	31	32	33	34	35	36
DIMM numbers (processor 4)	37	38	39	40	41	42	43	44	45	46	47	48

Memory sparing guidelines:

- The spare rank must have identical or larger memory capacity than all of the other active memory ranks on the same channel.
- If installing DIMMs that are one rank, follow the population sequences listed below.
- If installing DIMMs with more than one rank, follow population sequences specified for independent memory mode. See “Independent memory mode” on page 4.

The memory sparing DIMM population sequences for each supported processor configuration are:

- “Installation order: memory sparing with two processors” on page 16
- “Installation order: memory sparing with four processors” on page 17

Installation order: memory sparing with two processors

Memory module installation order for memory sparing with two processors installed in the compute node.

The following table shows the DIMM population sequence for memory sparing when two processors are installed.

Notes:

- An even number of DIMMs is required for memory sparing.
- There are two tables for memory sparing mode with two processors:
  - For single rank (1R) memory: Table 17 “Memory sparing with two processors for single rank (1R) memory” on page 16
  - For dual (2R) or higher rank memory: Table 18 “Memory sparing with two processors for dual (2R) or higher rank memory” on page 16

Table 17. Memory sparing with two processors for single rank (1R) memory

Total	Processor 1												Processor 2												Total
DIMMs	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	DIMMs
4					5	6											17	18							4
8					5	6	7	8									17	18	19	20					8
12			3	4	5	6	7	8							15	16	17	18	19	20					12
16			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			16
20	1	2	3	4	5	6	7	8	9	10			13	14	15	16	17	18	19	20	21	22			20
24	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	24

Table 18. Memory sparing with two processors for dual (2R) or higher rank memory

Total	Processor 1												Processor 2												Total
DIMMs	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	DIMMs
2					5												17								2
4					5			8									17			20					4
6			3		5			8							15		17			20					6
8			3		5			8		10					15		17			20		22			8
10	1		3		5			8		10			13		15		17			20		22			10
12	1		3		5			8		10		12	13		15		17			20		22		24	12
14			3	4	5	6		8		10		12			15	16	17	18		20		22		24	14
16			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			16
18	1	2	3	4	5	6		8		10		12	13	14	15	16	17	18		20		22		24	18
20	1	2	3	4	5	6	7	8	9	10			13	14	15	16	17	18	19	20	21	22			20
22	1	2	3	4	5	6	7	8	9	10		12	13	14	15	16	17	18	19	20	21	22		24	22
24	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	24

Installation order: memory sparing with four processors

Memory module installation order for memory sparing with four processors installed in the compute node.

There are two sections for memory sparing mode with four processors:

- For single rank (1R) memory: “Memory sparing with four processors for single rank (1R) memory” on page 17.
- For dual (2R) or higher rank memory: “Memory sparing with four processors for dual (2R) or higher rank memory” on page 18.

Memory sparing with four processors for single rank (1R) memory

The following tables show the DIMM population sequence for memory sparing when four processors are installed.

Note: When adding one or more DIMMs during a memory upgrade, you might need to move other DIMMs that are already installed to new locations.

Table 19. Memory sparing with four processors for single rank (1R) memory (Processors 1 and 2, 8 to 48 total DIMMs installed in compute node)

Total	Processor 1												Processor 2												Total
DIMMs	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	DIMMs
8					5	6											17	18							8
16					5	6	7	8									17	18	19	20					16
24			3	4	5	6	7	8							15	16	17	18	19	20					24
32			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			32
40	1	2	3	4	5	6	7	8	9	10			13	14	15	16	17	18	19	20	21	22			40
48	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	48

To continue populating processor 3 and 4 DIMMs for a system with 8 to 48 DIMMs, see Table 20 “Memory sparing with four processors for single rank (1R) memory (Processors 1 and 2, 8 to 48 total DIMMs installed in compute node)” on page 17.

Table 20. Memory sparing with four processors for single rank (1R) memory (Processors 1 and 2, 8 to 48 total DIMMs installed in compute node)

Total	Processor 3												Processor 4												Total
DIMMs	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	DIMMs
8							31	32											43	44					8
16					29	30	31	32									41	42	43	44					16
24					29	30	31	32	33	34							41	42	43	44	45	46			24
32			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			32
40			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	40
48	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	48

For processor 1 and 2 DIMM population sequences for systems with 8 to 48 DIMMs installed in compute node, see Table 19 “Memory sparing with four processors for single rank (1R) memory (Processors 1 and 2, 8 to 48 total DIMMs installed in compute node)” on page 17.

Memory sparing with four processors for dual (2R) or higher rank memory

Table 21. Memory sparing with four processors for dual (2R) or higher rank memory (Processors 1 and 2, 4 to 48 total DIMMs installed in compute node)

Total	Processor 1												Processor 2												Total
DIMMs	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	DIMMs
4					5												17								**4**
8					5			8									17			20					**8**
12			3		5			8							15		17			20					**12**
16			3		5			8		10					15		17			20		22			**16**
20	1		3		5			8		10			13		15		17			20		22			**20**
24	1		3		5			8		10		12	13		15		17			20		22		24	**24**
28			3	4	5	6		8		10		12			15	16	17	18		20		22		24	**28**
32			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**32**
36	1	2	3	4	5	6		8		10		12	13	14	15	16	17	18		20		22		24	**36**
40	1	2	3	4	5	6	7	8	9	10			13	14	15	16	17	18	19	20	21	22			**40**
44	1	2	3	4	5	6	7	8	9	10		12	13	14	15	16	17	18	19	20	21	22		24	**44**
48	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**48**

To continue populating processor 3 and 4 DIMMs for a system with 4 to 48 DIMMs, see Table 22 “Independent mode with four processors (Processors 3 and 4, 4 to 48 total DIMMs installed in compute node)” on page 19.

Table 22. Independent mode with four processors (Processors 3 and 4, 4 to 48 total DIMMs installed in compute node)

Total	Processor 3												Processor 4												Total
DIMMs	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	DIMMs
4								32												44					**4**
8					29			32									41			44					**8**
12					29			32		34							41			44		46			**12**
16			27		29			32		34					39		41			44		46			**16**
20			27		29			32		34		36			39		41			44		46		48	**20**
24	25		27		29			32		34		36	37		39		41			44		46		48	**24**
28	25		27		29		31	32	33	34			37		39		41		43	44	45	46			**28**
32			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			**32**
36	25		27		29		31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	**36**
40			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	**40**
44	25		27	28	29	30	31	32	33	34	35	36	37		39	40	41	42	43	44	45	46	47	48	**44**
48	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	**48**

For processor 1 and 2 DIMM population sequences for systems with 4 to 48 DIMMs installed in compute node, see Table 21 “Memory sparing with four processors for dual (2R) or higher rank memory (Processors 1 and 2, 4 to 48 total DIMMs installed in compute node)” on page 18.

Chapter 3. DC Persistent Memory Module (DCPMM) installation order

This section contains information of how to install DC Persistent Memory Module (DCPMM) and DRAM DIMMs.

For more information about the processors compatibility, see https://serverproven.lenovo.com/.

Notes:

- Before installing DCPMMs and DRAM DIMMs, refer to and make sure to meet all the requirements.
- To verify if the presently installed processors support DCPMMs, examine the four digits in the processor description. Only the processors with description meeting *both* of the following requirements support DCPMMs.
  - The first digit is ***5*** or a larger number.
  - The second digit is ***2***.

  Example: *Intel Xeon **52**15L* and *Intel Xeon Platinum **82**60M*

  If the installed processors do not support DCPMMs, replace them with those that do. For more details, see: https://www.intel.com/content/www/us/en/products/docs/memory-storage/optane-persistent-memory/lenovo-partner-video.html
- Supported memory capacity range varies with the following types of DCPMMs.
  - **Large memory tier (L):** The processors with **L** after the four digits (for example: *Intel Xeon 5215**L***) support up to 4.5 TB of memory capacity per processor
  - **Medium memory tier (M):** The processors with **M** after the four digits (for example: *Intel Xeon Platinum 8260**M***) support up to 2 TB of memory capacity per processor
  - **Other:** Other processors that support DCPMMs (for example: *Intel Xeon Gold 5222*) support up to 1 TB of memory capacity per processor

To install DC Persistent Memory (DCPMM), refer to the following combinations: “DC Persistent Memory Module — Memory Mode” on page 22

DC Persistent Memory Module — Memory Mode

In this mode, DCPMMs act as volatile system memory, while DRAM DIMMs act as cache. Only DCPMM capacity is displayed as system memory in this mode.

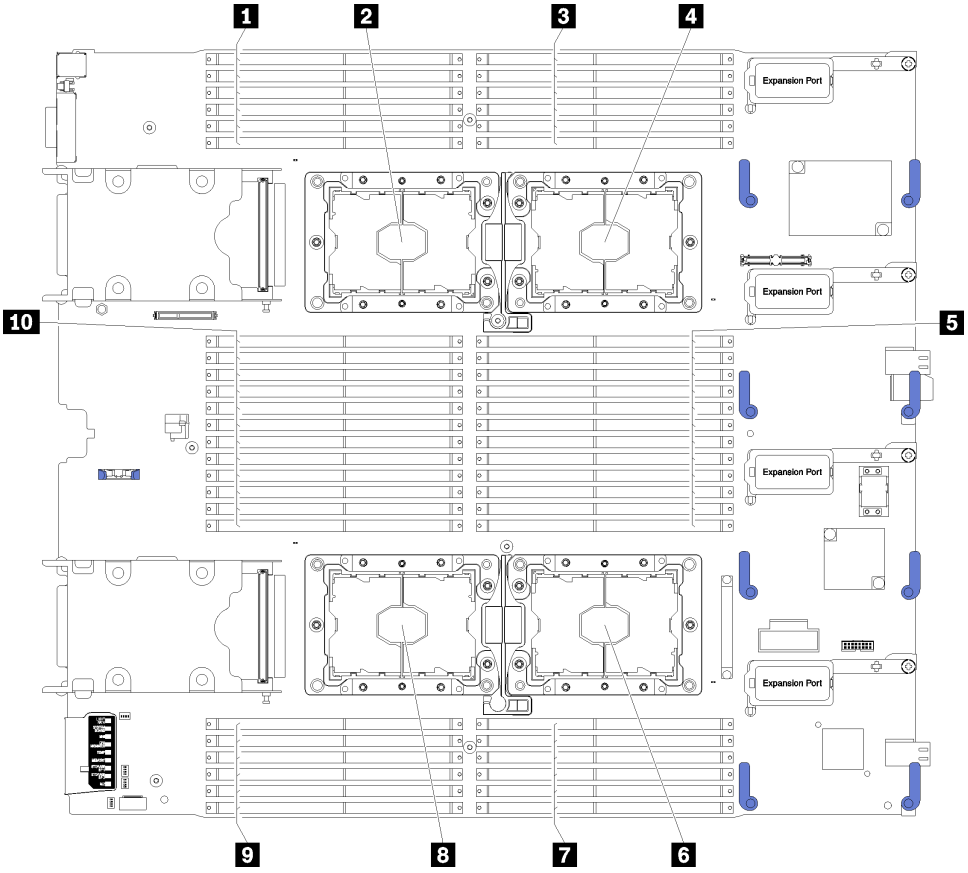

Figure 4. Processor and memory module layout

Table 23. Processor and memory module layout

1 DIMM 25 – 30	6 Processor socket 2
2 Processor socket 3	7 DIMM 19 – 24
3 DIMM 1 – 6	8 Processor socket 4
4 Processor socket 1	9 DIMM 43 – 48
5 DIMM 7 – 18	10 DIMM 31 – 42

Table 24. Channel and slot information of DIMMs around processor 1 and 2

Memory controllers	Controller 0						Controller 1					
Channels	Channel 2		Channel 1		Channel 0		Channel 0		Channel 1		Channel 2	
Slots	0	1	0	1	0	1	1	0	1	0	1	0
DIMM numbers (processor 1)	1	2	3	4	5	6	7	8	9	10	11	12
DIMM numbers (processor 2)	13	14	15	16	17	18	19	20	21	22	23	24

Table 25. Channel and slot information of DIMMs around processor 3 and 4

Memory controllers	Controller 1						Controller 0					
Channels	Channel 2		Channel 1		Channel 0		Channel 0		Channel 1		Channel 2	
Slots	0	1	0	1	0	1	1	0	1	0	1	0
DIMM numbers (processor 3)	25	26	27	28	29	30	31	32	33	34	35	36
DIMM numbers (processor 4)	37	38	39	40	41	42	43	44	45	46	47	48

The memory mode DIMM population sequences for each supported processor configuration are:

- “Installation order: Memory Mode with two processors” on page 24
- “Installation order: Memory Mode with four processors” on page 25

Installation order: Memory Mode with two processors

Memory module installation order for Memory Mode with two processors installed in the compute node.

The following table shows the DIMM population sequence for Memory Mode when two processors are installed.

Note: When adding one or more DIMMs during a memory upgrade, you might need to move other DIMMs that are already installed to new locations.

Table 26. Memory Mode with two processors

D: DRAM DIMMs with 16 GB or larger capacity.

P: Only DC Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
4 DCPMMs and 12 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
8 DCPMMs and 12 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
12 DCPMMs and 12 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D
4 DCPMMs and 8 DIMMs	**P**		D		D			D		D		**P**	**P**		D		D			D		D		**P**

Note: 4 DCPMMs and 8 DIMMs: one DIMM per processor channel configuration.

Table 27. Supported DCPMM capacity in Memory Mode with two processors

Total DCPMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	12	L		√	√
		M		√	√
		Other		√	
8	12	L	√	√	√
		M	√	√	
		Other	√		
12	12	L	√	√	√
		M	√	√	
		Other	√		
4	8	L	√	√	√
		M	√	√	√
		Other	√	√	

Installation order: Memory Mode with four processors

Memory module installation order for Memory Mode with four processors installed in the compute node.

The following tables show the DIMM population sequence for independent Memory Mode when four processors are installed.

Note: When adding one or more DIMMs during a memory upgrade, you might need to move other DIMMs that are already installed to new locations.

Table 28. Memory Mode with four processors (Processors 1 and 2)

D: DRAM DIMMs with 16 GB or larger capacity.

P: Only DC Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 1												Processor 2											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
8 DCPMMs and 24 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
16 DCPMMs and 24 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
24 DCPMMs and 24 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D
8 DCPMMs and 16 DIMMs	**P**		D		D			D		D		**P**	**P**		D		D			D		D		**P**

Note: 8 DCPMMs and 16 DIMMs: one DIMM per processor channel configuration.

Related DIMM population sequences for four processor systems:

To continue populating processor 3 and 4 DIMMs for system, see Table 29 “Memory Mode with four processors (Processors 3 and 4)” on page 26.

Table 29. Memory Mode with four processors (Processors 3 and 4)

D: DRAM DIMMs with 16 GB or larger capacity.

P: Only DC Persistent Memory Module (DCPMM) can be installed on the corresponding DIMM slots.

Configuration	Processor 3												Processor 4											
	25	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**	**48**
8 DCPMMs and 24 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
16 DCPMMs and 24 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
24 DCPMMs and 24 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D
8 DCPMMs and 16 DIMMs	**P**		D		D			D		D		**P**	**P**		D		D			D		D		**P**

Note: 8 DCPMMs and 16 DIMMs: one DIMM per processor channel configuration.

Related DIMM population sequences for four processor systems:

To continue populating processor 1 and 2 DIMMs for system, see Table 28 “Memory Mode with four processors (Processors 1 and 2)” on page 25.

Table 30. Supported DCPMM capacity in Memory Mode with four processors

Total DCPMMs	**Total DIMMs**	**Processor Family**	**128 GB DCPMM**	**256 GB DCPMM**	**512 GB DCPMM**
8	**24**	**L**		√	√
		M		√	√
		Other		√	
16	**24**	**L**	√	√	√
		M	√	√	
		Other	√		
24	**24**	**L**	√	√	√
		M	√	√	
		Other	√		
8	**16**	**L**	√	√	√
		M	√	√	√
		Other	√	√	

Index

D

G

I

M

N

Lenovo

Part Number: SP47A27061

Printed in China

(1P) P/N: SP47A27061