ThinkSystem SR860
Memory Population Reference

Machine Types: 7X69 and 7X70

Note

Before using this information and the product it supports, be sure to read and understand the safety information and the safety instructions, which are available at:https://pubs.lenovo.com/safety_documentation/

In addition, be sure that you are familiar with the terms and conditions of the Lenovo warranty for your server, which can be found at:http://datacentersupport.lenovo.com/warrantylookup

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Chapter 1. Memory module installation guideline

There are a number of criteria that must be followed when selecting and installing memory modules in your server.

Memory installation requirements:

- A label on each DIMM identifies the DIMM type. This information is in the format **xxxxx *n*Rxxx PC4-xxxxx-xx-xx-xxx**. Where ***n*** indicates if the DIMM is single-rank (n=1) or dual-rank (n=2).
- At least one DIMM is required for each processor. Install at least six DIMMs per processor for good performance.
- The following table includes all the feasible combinations of different types of DIMMs:

Table 1. DIMM compatibility

DIMM Types	RDIMM	LRDIMM	3DS-RDIMM
RDIMM	V	X	X
LRDIMM	X	V	X
3DS-RDIMM	X	X	V

- When you replace a DIMM, the server provides automatic DIMM enablement capability without requiring you to use the Setup utility to enable the new DIMM manually.

Attention:

- Mixing x4 and x8 DIMMs in the same channel is allowed.
- Install DIMMs of the same speed for optimal performance. Otherwise, the BIOS will find and run the lowest speed among all channels.
- Always populate DIMMs with the maximum number of ranks in the farthest DIMM slot, followed by the nearest DIMM slot.

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Chapter 2. Memory module installation rules and order

Memory modules must be installed in a specific order based on the memory configuration that you implement and the number of processors and memory modules installed in the server.

The following memory configurations and population sequences are supported for the ThinkSystem SR860 server:

- "Independent memory mode" on page 4
  - "Installation order: independent memory mode with two processors" on page 7
  - "Installation order: independent memory mode with four processors" on page 8
- "Memory mirroring" on page 12
  - "Installation order: memory mirroring with two processors" on page 14
  - "Installation order: memory mirroring with four processors" on page 15
- "Memory sparing" on page 17
  - "Installation order: memory sparing with two processors" on page 20
  - "Installation order: memory sparing with four processors" on page 21

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Independent memory mode

In independent memory mode, memory channels can be populated with DIMMs in any order and you can populate all channels for each processor in any order with no matching requirements. Independent memory mode provides the highest level of memory performance, but lacks failover protection. The DIMM installation order for independent memory mode varies based on the number of processors and memory modules installed in the server.

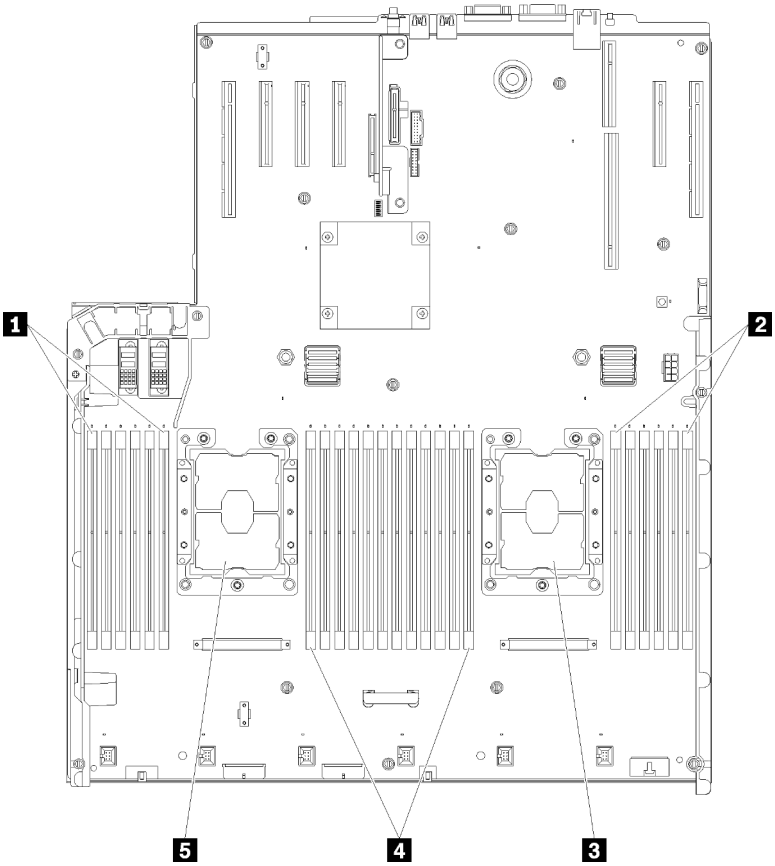

Figure 1. Processor and memory module layout: processor 1 and 2

Table 2. Processor and memory module layout: processor 1 and 2

1 DIMM 1-6	4 DIMM 7-18
2 DIMM 19-24	5 Processor 1
3 Processor 2	

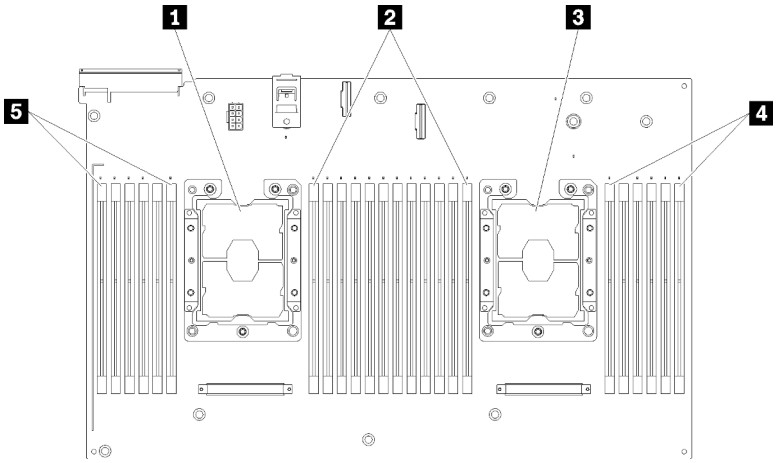

Figure 2. Processor and memory module layout: processor 3 and 4

Table 3. Processor and memory module layout: processor 3 and 4

1 Processor 3	4 DIMM 43-48
2 DIMM 31-42	5 DIMM 25-30
3 Processor 4	

Table 4. Channel and slot information of DIMMs around a processor

Slot	0	1	0	1	0	1		1	0	1	0	1	0
Channel	Channel 2		Channel 1		Channel 0			Channel 0		Channel 1		Channel 2	
DIMM number (Processor 1)	1	2	3	4	5	6		7	8	9	10	11	12
DIMM number (Processor 2)	13	14	15	16	17	18	Processor	19	20	21	22	23	24
DIMM number (Processor 3)	25	26	27	28	29	30		31	32	33	34	35	36
DIMM number (Processor 4)	37	38	39	40	41	42		43	44	45	46	47	48

Independent memory mode guidelines:

- Individual memory channels can run at different DIMM timings, but all channels must run at the same interface frequency.
- Populate memory channel 0 first.
- Memory channel 1 is empty or identically populated as memory channel 0.
- Memory channel 2 is empty or identically populated as memory channel 1.
- In each memory channel, populate slot 0 first.
- If a memory channel has two DIMMs, populate the DIMM with a higher number of ranks in slot 0.

The independent memory mode DIMM population sequences for each supported processor configuration are:

- "Installation order: independent memory mode with two processors" on page 7
- "Installation order: independent memory mode with four processors" on page 8

Installation order: independent memory mode with two processors

Memory module installation order for independent (non-mirroring) memory mode with two processors installed in the server.

The following table shows the DIMM population sequence for independent memory mode when two processors are installed.

- Processors 1 and 2 are installed on the system board.

Note: When adding one or more DIMMs during a memory upgrade, you might need to remove some DIMMs that are already installed to new locations.

Table 5. Independent mode with two processors

Total	Processor 1												Processor 2												Total
DIMMs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**DIMMs**
2								8												20					**2**
3					5			8												20					**3**
4					5			8									17			20					**4**
5					5			8		10							17			20					**5**
6					5			8		10							17			20		22			**6**
7			3		5			8		10							17			20		22			**7**
8			3		5			8		10					15		17			20		22			**8**
9			3		5			8		10		12			15		17			20		22			**9**
10			3		5			8		10		12			15		17			20		22		24	**10**
11	1		3		5			8		10		12			15		17			20		22		24	**11**
12	1		3		5			8		10		12	13		15		17			20		22		24	**12**
13	1		3		5		7	8	9	10			13		15		17			20		22		24	**13**
14	1		3		5		7	8	9	10			13		15		17		19	20	21	22			**14**
15			3	4	5	6	7	8	9	10			13		15		17		19	20	21	22			**15**
16			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**16**
17	1		3		5		7	8	9	10	11	12			15	16	17	18	19	20	21	22			**17**
18	1		3		5		7	8	9	10	11	12	13		15		17		19	20	21	22	23	24	**18**
19			3	4	5	6	7	8	9	10	11	12	13		15		17		19	20	21	22	23	24	**19**
20			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	**20**
21	1	2	3	4	5	6	7	8	9	10	11	12	13		15		17		19	20	21	22	23	24	**21**
22	1		3	4	5	6	7	8	9	10	11	12	13		15	16	17	18	19	20	21	22	23	24	**22**
23	1	2	3	4	5	6	7	8	9	10	11	12	13		15	16	17	18	19	20	21	22	23	24	**23**
24	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**24**

Installation order: independent memory mode with four processors

Memory module installation order for independent (non-mirroring) memory mode with four processors installed in the server.

The following tables show the DIMM population sequence for independent memory mode when four processors are installed.

- Processors 1 and 2 are installed on the system board.
- Processors 3 and 4 are installed in the processor and memory expansion tray.

Note: When adding one or more DIMMs during a memory upgrade, you might need to remove some DIMMs that are already installed to new locations.

Table 6. Independent mode with four processors (Processor 1 and 2, 4 to 24 total DIMMs installed in server)

Total	Processor 1												Processor 2												Total
DIMMs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**DIMMs**
4								8												20					**4**
5					5			8												20					**5**
6					5			8									17			20					**6**
7					5			8									17			20					**7**
8					5			8									17			20					**8**
9					5			8		10							17			20					**9**
10					5			8		10							17			20		22			**10**
11					5			8		10							17			20		22			**11**
12					5			8		10							17			20		22			**12**
13			3		5			8		10							17			20		22			**13**
14			3		5			8		10					15		17			20		22			**14**
15			3		5			8		10					15		17			20		22			**15**
16			3		5			8		10					15		17			20		22			**16**
17			3		5			8		10		12			15		17			20		22			**17**
18			3		5			8		10		12			15		17			20		22		24	**18**
19			3		5			8		10		12			15		17			20		22		24	**19**
20			3		5			8		10		12			15		17			20		22		24	**20**
21	1		3		5			8		10		12			15		17			20		22		24	**21**
22	1		3		5			8		10		12	13		15		17			20		22		24	**22**
23	1		3		5			8		10		12	13		15		17			20		22		24	**23**
24	1		3		5			8		10		12	13		15		17			20		22		24	**24**

Related DIMM population sequences for four processor systems:

- Processor 1 and 2 DIMM population sequence for 25 to 48 DIMMs, see Table 7 “Independent mode with four processors (Processor 1 and 2, 25 to 48 total DIMMs installed in server)” on page 9.
- To continue populating processor 3 and 4 DIMMs for a system with 4 to 24 DIMMs, see Table 8 “Independent mode with four processors (Processor 3 and 4, 4 to 24 total DIMMs installed in server)” on page 10.

Table 7. Independent mode with four processors (Processor 1 and 2, 25 to 48 total DIMMs installed in server)

Total	Processor 1												Processor 2												Total
DIMMs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**DIMMs**
25	1		3		5		7	8	9	10			13		15		17			20		22		24	**25**
26	1		3		5		7	8	9	10			13		15		17		19	20	21	22			**26**
27	1		3		5		7	8	9	10			13		15		17		19	20	21	22			**27**
28	1		3		5		7	8	9	10			13		15		17		19	20	21	22			**28**
29			3	4	5	6	7	8	9	10			13		15		17		19	20	21	22			**29**
30			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**30**
31			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**31**
32			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**32**
33	1		3		5		7	8	9	10	11	12			15	16	17	18	19	20	21	22			**33**
34	1		3		5		7	8	9	10	11	12	13		15		17		19	20	21	22	23	24	**34**
35	1		3		5		7	8	9	10	11	12	13		15		17		19	20	21	22	23	24	**35**
36	1		3		5		7	8	9	10	11	12	13		15		17		19	20	21	22	23	24	**36**
37			3	4	5	6	7	8	9	10	11	12	13		15		17		19	20	21	22	23	24	**37**
38			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	**38**
39			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	**39**
40			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	**40**
41	1	2	3	4	5	6	7	8	9	10	11	12	13		15		17		19	20	21	22	23	24	**41**
42	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**42**
43	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**43**
44	1		3	4	5	6	7	8	9	10	11	12	13		15	16	17	18	19	20	21	22	23	24	**44**
45	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**45**
46	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**46**
47	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**47**
48	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**48**

Related DIMM population sequences for four processor systems:

- Processor 1 and 2 DIMM population sequence for 4 to 24 DIMMs, see Table 6 “Independent mode with four processors (Processor 1 and 2, 4 to 24 total DIMMs installed in server)” on page 8.
- To continue populating processor 3 and 4 DIMMs for a system with 25 to 48 DIMMs, see Table 9 “Independent mode with four processors (Processor 3 and 4, 25 to 48 total DIMMs installed in server)” on page 11.

Table 8. Independent mode with four processors (Processor 3 and 4, 4 to 24 total DIMMs installed in server)

Total	Processor 3												Processor 4												Total
DIMMs	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**	**48**	**DIMMs**
4								32												44					**4**
5								32												44					**5**
6								32												44					**6**
7					29			32												44					**7**
8					29			32									41			44					**8**
9					29			32									41			44					**9**
10					29			32									41			44					**10**
11					29			32		34							41			44					**11**
12					29			32		34							41			44		46			**12**
13					29			32		34							41			44		46			**13**
14					29			32		34							41			44		46			**14**
15			27		29			32		34							41			44		46			**15**
16			27		29			32		34					39		41			44		46			**16**
17			27		29			32		34					39		41			44		46			**17**
18			27		29			32		34					39		41			44		46			**18**
19			27		29			32		34		36			39		41			44		46			**19**
20			27		29			32		34		36			39		41			44		46		48	**20**
21			27		29			32		34		36			39		41			44		46		48	**21**
22			27		29			32		34		36			39		41			44		46		48	**22**
23	25		27		29			32		34		36			39		41			44		46		48	**23**
24	25		27		29			32		34		36	37		39		41			44		46		48	**24**

Related DIMM population sequences for four processor systems:

- Processor 3 and 4 DIMM population sequence for 25 to 48 DIMMs, see Table 9 “Independent mode with four processors (Processor 3 and 4, 25 to 48 total DIMMs installed in server)” on page 11.
- To continue populating processor 1 and 2 DIMMs for a system with 4 to 24 DIMMs, see Table 6 “Independent mode with four processors (Processor 1 and 2, 4 to 24 total DIMMs installed in server)” on page 8.

Table 9. Independent mode with four processors (processor 3 and 4, 25 to 48 total DIMMs installed in server)

Total	Processor 3												Processor 4												Total
DIMMs	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**	**48**	**DIMMs**
25	25		27		29			32		34		36	37		39		41			44		46		48	**25**
26	25		27		29			32		34		36	37		39		41			44		46		48	**26**
27	25		27		29		31	32	33	34			37		39		41			44		46		48	**27**
28	25		27		29		31	32	33	34			37		39		41		43	44	45	46			**28**
29	25		27		29		31	32	33	34			37		39		41		43	44	45	46			**29**
30	25		27		29		31	32	33	34			37		39		41		43	44	45	46			**30**
31			27	28	29	30	31	32	33	34			37		39		41		43	44	45	46			**31**
32			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			**32**
33			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			**33**
34			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			**34**
35	25		27		29		31	32	33	34	35	36			39	40	41	42	43	44	45	46			**35**
36	25		27		29		31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	**36**
37	25		27		29		31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	**37**
38	25		27		29		31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	**38**
39			27	28	29	30	31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	**39**
40			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	**40**
41			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	**41**
42	25		27		29		31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	**42**
43			27	28	29	30	31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	**43**
44	25		27	28	29	30	31	32	33	34	35	36	37		39	40	41	42	43	44	45	46	47	48	**44**
45	25	26	27	28	29	30	31	32	33	34	35	36	37		39		41		43	44	45	46	47	48	**45**
46	25	26	27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	**46**
47	25	26	27	28	29	30	31	32	33	34	35	36	37		39	40	41	42	43	44	45	46	47	48	**47**
48	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	**48**

Related DIMM population sequences for four processor systems:

- Processor 3 and 4 DIMM population sequence for 4 to 24 DIMMs, see Table 8 “Independent mode with four processors (Processor 3 and 4, 4 to 24 total DIMMs installed in server)” on page 10.
- To continue populating processor 1 and 2 DIMMs for a system with 25 to 48 DIMMs, see Table 7 “Independent mode with four processors (Processor 1 and 2, 25 to 48 total DIMMs installed in server)” on page 9.

Memory mirroring

Memory-mirroring mode provides full memory redundancy while reducing the total system memory capacity in half. Memory channels are grouped in pairs with each channel receiving the same data. If a failure occurs, the memory controller switches from the DIMMs on the primary channel to the DIMMs on the backup channel. The DIMM installation order for memory mirroring varies based on the number of processors and DIMMs installed in the server.

Memory mirroring guidelines:

- Memory mirroring reduces the maximum available memory by half of the installed memory. For example, if the server has 64 GB of installed memory, only 32 GB of addressable memory is available when memory mirroring is enabled.
- Each DIMM must be identical in size and architecture.
- DIMMs on each memory channel must be of equal density.
- If two memory channels have DIMMs, mirroring occurs across two DIMMs (channels 0/1 will both contain the primary/secondary memory caches).
- If three memory channels have DIMMs, mirroring occurs across all three DIMMs (channels 0/1, channels 1/2, and channels 2/0 will all contain primary/secondary memory caches).

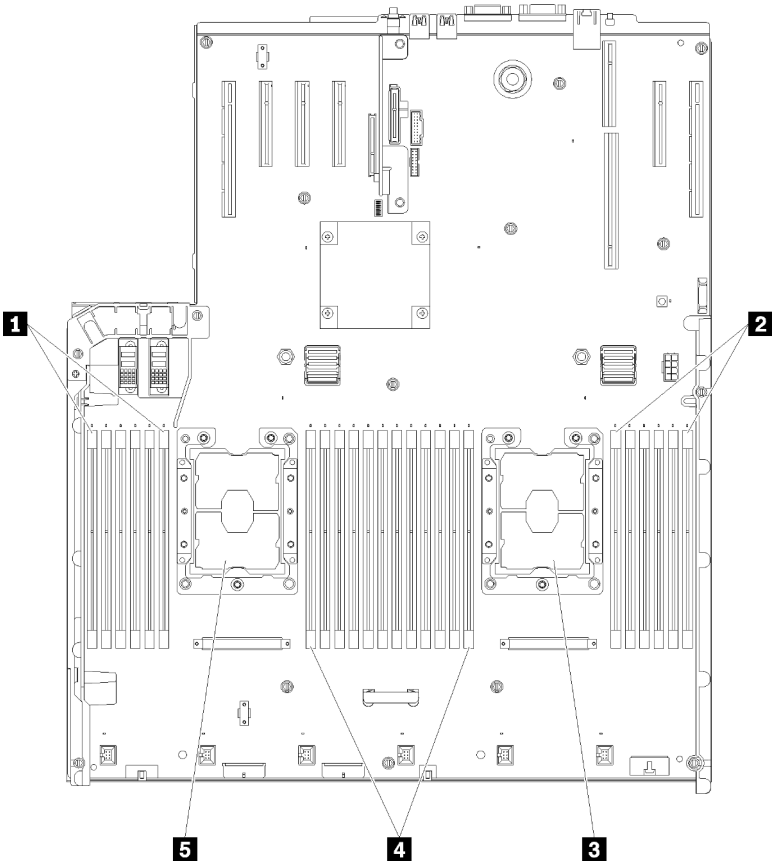

Figure 3. Processor and memory module layout: processor 1 and 2

Table 10. Processor and memory module layout: processor 1 and 2

1 DIMM 1-6	4 DIMM 7-18
2 DIMM 19-24	5 Processor 1
3 Processor 2	

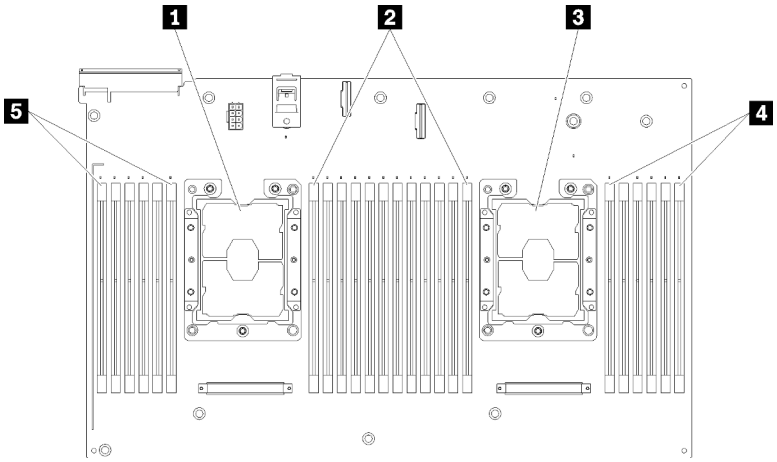

Figure 4. Processor and memory module layout: processor 3 and 4

Table 11. Processor and memory module layout: processor 3 and 4

1 Processor 3	4 DIMM 43-48
2 DIMM 31-42	5 DIMM 25-30
3 Processor 4	

Table 12. Channel and slot information of DIMMs around a processor

Slot	0	1	0	1	0	1	Processor	1	0	1	0	1	0
Channel	Channel 2		Channel 1		Channel 0			Channel 0		Channel 1		Channel 2	
DIMM number (Processor 1)	1	2	3	4	5	6		7	8	9	10	11	12
DIMM number (Processor 2)	13	14	15	16	17	18		19	20	21	22	23	24
DIMM number (Processor 3)	25	26	27	28	29	30		31	32	33	34	35	36
DIMM number (Processor 4)	37	38	39	40	41	42		43	44	45	46	47	48

Memory mirroring DIMM population sequences for each of the supported processor configurations is shown by one of the following topics:

- "Installation order: memory mirroring with two processors" on page 14
- "Installation order: memory mirroring with four processors" on page 15

Installation order: memory mirroring with two processors

Memory module installation order for memory mirroring with two processors installed in the server.

The following table shows the DIMM population sequence for memory mirroring when two processors are installed.

- Processors 1 and 2 are installed on the system board.

Note: When adding one or more DIMMs during a memory upgrade, you might need to remove some DIMMs that are already installed to new locations.

Table 13. Memory mirroring with two processors

Total	Processor 1												Processor 2												Total
DIMMs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**DIMMs**
4								8		10										20		22			**4**
5								8		10		12								20		22			**5**
6								8		10		12								20		22		24	**6**
7			3		5			8		10										20		22		24	**7**
8			3		5			8		10					15		17			20		22			**8**
9	1		3		5			8		10		12								20		22		24	**9**
10	1		3		5			8		10		12			15		17			20		22			**10**
12	1		3		5			8		10		12	13		15		17			20		22		24	**12**
13	1		3		5		7	8	9	10	11	12			15		17			20		22			**13**
14	1		3		5			8		10		12			15	16	17	18	19	20	21	22			**14**
15	1		3		5		7	8	9	10	11	12	13		15		17			20		22		24	**15**
16			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**16**
17	1		3		5		7	8	9	10	11	12			15	16	17	18	19	20	21	22			**17**
18	1	2	3	4	5	6	7	8	9	10	11	12	13		15		17			20		22		24	**18**
20	1	2	3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22			**20**
21	1	2	3	4	5	6	7	8	9	10	11	12	13		15		17		19	20	21	22	23	24	**21**
24	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**24**

Installation order: memory mirroring with four processors

Memory module installation order for memory mirroring with four processors installed in the server.

The following tables show the DIMM population sequence for memory mirroring when four processors are installed.

- Processors 1 and 2 are installed on the system board.
- Processors 3 and 4 are installed in the processor and memory expansion tray.

Note: When adding one or more DIMMs during a memory upgrade, you might need to remove some DIMMs that are already installed to new locations.

Table 14. Memory mirroring with four processors (Processors 1 and 2)

Total	Processor 1												Processor 2												Total
DIMMs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**DIMMs**
8								8		10										20		22			**8**
10								8		10		12								20		22			**10**
12			3		5			8		10										20		22			**12**
14			3		5			8		10										20		22		24	**14**
16			3		5			8		10					15		17			20		22			**16**
18	1		3		5			8		10		12			15		17			20		22			**18**
20	1		3		5			8		10		12			15		17			20		22			**20**
22	1		3		5			8		10		12	13		15		17			20		22		24	**22**
24	1		3		5			8		10		12	13		15		17			20		22		24	**24**
26			3	4	5	6	7	8	9	10			13		15		17			20		22		24	**26**
28			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**28**
30			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**30**
32			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**32**
34	1	2	3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22			**34**
36	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**36**
38	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**38**
40	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**40**
42	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**42**
44	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**44**
48	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**48**

Related DIMM population sequences for four processor systems:

- To continue populating processor 3 and 4 DIMMs, see Table 15 “Memory mirroring with four processors (Processor 3 and 4)” on page 16.

Table 15. Memory mirroring with four processors (processor 3 and 4)

Total	Processor 3												Processor 4												Total
DIMMs	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**	**48**	**DIMMs**
8								32		34										44		46			**8**
10								32		34		36								44		46			**10**
12			27		29			32		34										44		46			**12**
14			27		29			32		34										44		46		48	**14**
16			27		29			32		34					39		41			44		46			**16**
18			27		29			32		34					39		41			44		46			**18**
20	25		27		29			32		34		36			39		41			44		46			**20**
22	25		27		29			32		34		36			39		41			44		46			**22**
24	25		27		29			32		34		36	37		39		41			44		46		48	**24**
26	25		27		29			32		34		36	37		39		41			44		46		48	**26**
28	25		27		29			32		34		36	37		39		41			44		46		48	**28**
30			27	28	29	30	31	32	33	34			37		39		41			44		46		48	**30**
32			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			**32**
34			27	28	29	30	31	32	33	34			37		39		41			44		46		48	**34**
36	25		27		29			32		34		36	37		39		41			44		46		48	**36**
38			27	28	29	30	31	32	33	34			37		39		41			44		46		48	**38**
40			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			**40**
42	25	26	27	28	29	30	31	32	33	34	35	36	37		39		41			44		46		48	**42**
44	25	26	27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	**44**
48	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	10	41	42	43	44	45	46	47	48	**48**

Related DIMM population sequences for four processor systems:

- To continue populating processor 1 and 2 DIMMs, see Table 14 “Memory mirroring with four processors (Processor 1 and 2)” on page 15.

Memory sparing

In memory-sparing mode, one memory rank serves as a spare for other ranks on the same channel in case they fail. The spare rank is held in reserve and not used as active memory until a failure is indicated, with reserved capacity subtracted from the total available memory in the system. The DIMM installation order for memory sparing varies based on the number of processors and memory modules installed in the server.

After an error threshold is surpassed in a system protected by memory sparing, the content of a failing rank of DIMMs is copied to the spare rank. The failing rank is then taken offline and the spare rank placed online for use as active memory in place of the failed rank. Since the failover process involves copying of memory content, the level of memory redundancy provided by memory sparing is less than that provided by memory mirroring: memory mirroring is the preferred failure-protection choice for critical applications.

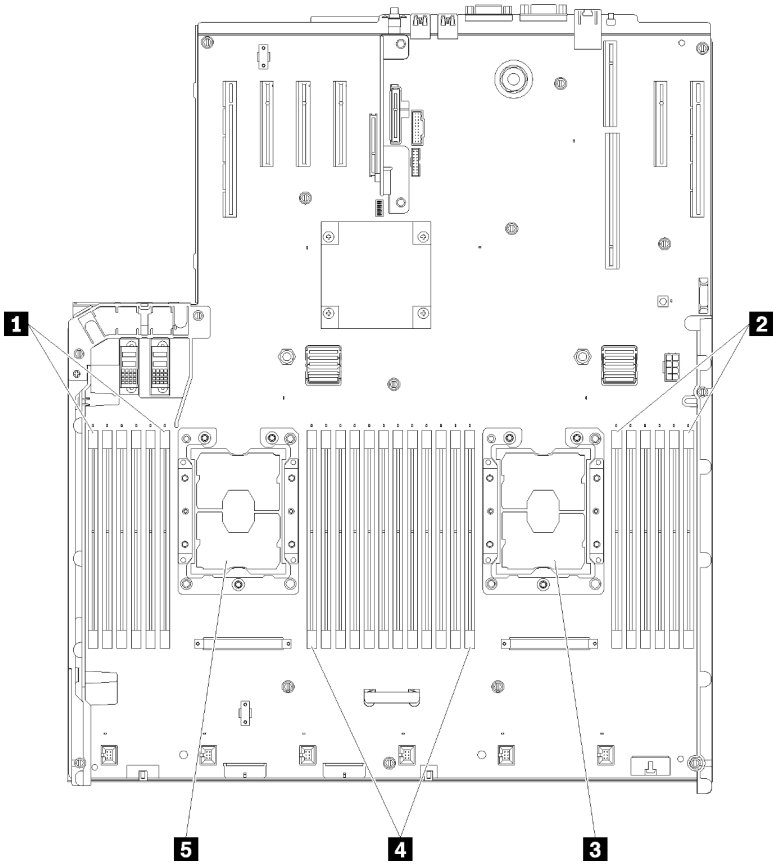

Figure 5. Processor and memory module layout: processor 1 and 2

Table 16. Processor and memory module layout: processor 1 and 2

1 DIMM 1-6	4 DIMM 7-18
2 DIMM 19-24	5 Processor 1
3 Processor 2	

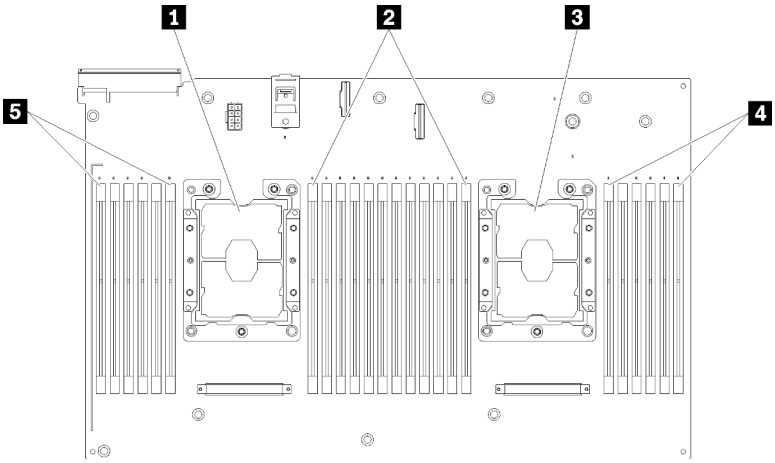

Figure 6. Processor and memory module layout: processor 3 and 4

Table 17. Processor and memory module layout: processor 3 and 4

1 Processor 3	4 DIMM 43-48
2 DIMM 31-42	5 DIMM 25-30
3 Processor 4	

Table 18. Channel and slot information of DIMMs around a processor

Slot	0	1	0	1	0	1		1	0	1	0	1	0
Channel	Channel 2		Channel 1		Channel 0			Channel 0		Channel 1		Channel 2	
DIMM number (Processor 1)	1	2	3	4	5	6		7	8	9	10	11	12
DIMM number (Processor 2)	13	14	15	16	17	18	Processor	19	20	21	22	23	24
DIMM number (Processor 3)	25	26	27	28	29	30		31	32	33	34	35	36
DIMM number (Processor 4)	37	38	39	40	41	42		43	44	45	46	47	48

Memory sparing guidelines:

- The spare rank must have identical or larger memory capacity than all of the other active memory ranks on the same channel.
- If installing DIMMs that are one rank, follow the population sequences listed below.
- If installing DIMMs with more than one rank, follow population sequences specified for independent memory mode. See "Independent memory mode" on page 4.

The memory sparing DIMM population sequences for each supported processor configuration are:

- "Installation order: memory sparing with two processors" on page 20
- "Installation order: memory sparing with four processors" on page 21

Note: This mode only applies to single-rank memory modules. When installing DIMMs consisting of more than two ranks, including dual-rank, quad-rank or octal-rank memory modules, refer to "Independent memory mode" on page 4 instead.

Installation order: memory sparing with two processors

Memory module installation order for memory sparing with two processors installed in the server.

The following table shows the DIMM population sequence for memory sparing when two processors are installed.

- Processors 1 and 2 are installed on the system board.

Notes:

1. An even number of DIMMs is required for memory sparing.
2. This mode only applies to single-rank memory modules. When installing DIMMs consisting of more than two ranks, including dual-rank, quad-rank or octal-rank memory modules, refer to "Independent memory mode" on page 4 instead.

Table 19. Memory sparing with two processors

Total	Processor 1												Processor 2												Total
DIMMs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**DIMMs**
4							7	8											19	20					**4**
6					5	6	7	8											19	20					**6**
8					5	6	7	8									17	18	19	20					**8**
10					5	6	7	8	9	10							17	18	19	20					**10**
12					5	6	7	8	9	10							17	18	19	20	21	22			**12**
14			3	4	5	6	7	8	9	10							17	18	19	20	21	22			**14**
16			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**16**
18			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22			**18**
20			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	**20**
22	1	2	3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	**22**
24	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**24**

Installation order: memory sparing with four processors

Memory module installation order for memory sparing with four processors installed in the server.

The following tables show the DIMM population sequence for memory sparing when four processors are installed.

- Processors 1 and 2 are installed on the system board.
- Processors 3 and 4 are installed in the processor and memory expansion tray.

Notes:

1. When adding one or more DIMMs during a memory upgrade, you might need to remove some DIMMs that are already installed to new locations.
2. An even number of DIMMs is required for memory sparing.
3. This mode only applies to single-rank memory modules. When installing DIMMs consisting of more than two ranks, including dual-rank, quad-rank or octal-rank memory modules, refer to "Independent memory mode" on page 4 instead.

Table 20. Memory sparing with four processors (processor 1 and 2)

Total	Processor 1												Processor 2												Total
DIMMs	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**DIMMs**
8							7	8											19	20					**8**
10					5	6	7	8											19	20					**10**
12					5	6	7	8									17	18	19	20					**12**
14					5	6	7	8									17	18	19	20					**14**
16					5	6	7	8									17	18	19	20					**16**
18					5	6	7	8	9	10							17	18	19	20					**18**
20					5	6	7	8	9	10							17	18	19	20	21	22			**20**
22					5	6	7	8	9	10							17	18	19	20	21	22			**22**
24					5	6	7	8	9	10							17	18	19	20	21	22			**24**
26			3	4	5	6	7	8	9	10							17	18	19	20	21	22			**26**
28			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**28**
30			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**30**
32			3	4	5	6	7	8	9	10					15	16	17	18	19	20	21	22			**32**
34			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22			**34**
36			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	**36**
38			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	**38**
40			3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	**40**
42	1	2	3	4	5	6	7	8	9	10	11	12			15	16	17	18	19	20	21	22	23	24	**42**
44	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**44**
46	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**46**
48	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	**48**

Related DIMM population sequences for four processor systems:

- To continue populating processor 3 and 4 DIMMs, see Table 21 "Memory sparing with four processors (processor 3 and 4)" on page 23.

Table 21. Memory mirroring with four processors (processor 3 and 4)

Total	Processor 3												Processor 4												Total
DIMMs	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**	**48**	**DIMMs**
8							31	32											43	44					**8**
10							31	32											43	44					**10**
12							31	32											43	44					**12**
14					29	30	31	32											43	44					**14**
16					29	30	31	32									41	42	43	44					**16**
18					29	30	31	32									41	42	43	44					**18**
20					29	30	31	32									41	42	43	44					**20**
22					29	30	31	32	33	34							41	42	43	44					**22**
24					29	30	31	32	33	34							41	42	43	44	45	46			**24**
26					29	30	31	32	33	34							41	42	43	44	45	46			**26**
28					29	30	31	32	33	34							41	42	43	44	45	46			**28**
30			27	28	29	30	31	32	33	34							41	42	43	44	45	46			**30**
32			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			**32**
34			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			**34**
36			27	28	29	30	31	32	33	34					39	40	41	42	43	44	45	46			**36**
38			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46			**38**
40			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	**40**
42			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	**42**
44			27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	**44**
46	25	26	27	28	29	30	31	32	33	34	35	36			39	40	41	42	43	44	45	46	47	48	**46**
48	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	**48**

Related DIMM population sequences for four processor systems:

- To continue populating processor 1 and 2 DIMMs, see Table 20 “Memory sparing with four processors (processors 1 and 2)” on page 21.

Chapter 3. DCPMM and DRAM DIMM installation order

This section contains information of how to install DCPMMs and DRAM DIMMs properly.

Notes:

- Before installing DCPMMs and DRAM DIMMs, refer to “DC Persistent Memory (DCPMM) setup” in *Setup Guide* and make sure to meet all the requirements.
- To verify if the presently installed processors support DCPMMs, examine the four digits in the processor description. Only the processor with description meeting *both* of the following requirements support DCPMMs.
  - The first digit is ***5*** or a larger number.

    Note: The only exception to this rule is *Intel Xeon Silver 4215*, which also supports DCPMM.
  - The second digit is ***2***.

  Example: *Intel Xeon **52**15L* and *Xeon Platinum **82**80M*

  To verify if the presently installed processors support DCPMMs, examine the four digits in the processor description. Only the processor with description meeting *both* of the following requirements support DCPMMs.
- Supported memory capacity range varies with the following types of DCPMMs.
  - **Large memory tier (L):** The processors with **L** after the four digits (for example: *Intel Xeon **52**15L*)
  - **Medium memory tier (M):** The processors with **M** after the four digits (for example: *Xeon Platinum **82**80M*)
  - **Other:** Other processors that support DCPMMs (for example: *Intel Xeon Gold 5222*)

In addition, you can take advantage of a memory configurator, which is available at the following site:

https://dcsc.lenovo.com/#/memory_configuration

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App Direct Mode

In this mode, DCPMMs act as independent and persistent memory resources directly accessible by specific applications, and DRAM DIMMs act as system memory.

Installation order: App Direct Mode with two processors

Memory module installation order for DCPMM App Direct Mode with two installed processors.

Table 22. Memory population in App Direct Mode with two processors

- **D: DRAM DIMMs with 16 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
4 DCPMMs and 8 DIMMs	**P**		D		D			D		D		**P**	**P**		D		D			D		D		**P**
4 DCPMMs and 16 DIMMs	**P**		D	D	D	D	D	D	D	D		**P**	**P**		D	D	D	D	D	D	D	D		**P**
4 DCPMMs and 12 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
8 DCPMMs and 12 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
12 DCPMMs and 12 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D

Table 23. Supported DCPMM capacity in App Direct Mode with two processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	8	L	√	√	√
		M	√	√	√
		Other	√	√	
4	16	L	√	√	√
		M	√	√	√
		Other	√	√	
4	12	L	√	√	√
		M	√	√	√
		Other	√	√	
8	12	L	√	√	√
		M	√	√	
		Other	√		
12	12	L	√	√	√
		M	√	√	

Table 23. Supported DCPMM capacity in App Direct Mode with two processors (continued)

		Other	√		

Table 24. Memory population in App Direct Mode with two processors (not interleaved only)

- **D: DRAM DIMMs with 16 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	**Processor 1**												**Processor 2**											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
1 DCPMM and 12 DIMMs	D		D		D		**P**	D		D		D	D		D		D			D		D		D
2 DCPMMs and 12 DIMMs	D		D		D		**P**	D		D		D	D		D		D		**P**	D		D		D

Table 25. Supported DCPMM capacity in App Direct Mode with two processors (not interleaved only)

Total PMMs	**Total DIMMs**	**Processor Family**	**128 GB DCPMM**	**256 GB DCPMM**	**512 GB DCPMM**
1	**12**	**L**	√	√	√
		M	√	√	√
		Other	√	√	√
2	**12**	**L**	√	√	√
		M	√	√	√
		Other	√	√	√

Installation order: App Direct Mode with four processors

Memory module installation order for DCPMM App Direct Mode with four installed processors.

Table 26. Memory population in App Direct Mode with four processors

- **D: DRAM DIMMs with 16 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	Processor 3												Processor 4											
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
8 DCPMMs and 16 DIMMs	**P**		D		D			D		D		**P**	**P**		D		D			D		D		**P**
8 DCPMMs and 32 DIMMs	**P**		D	D	D	D	D	D	D	D		**P**	**P**		D	D	D	D	D	D	D	D		**P**
8 DCPMMs and 24 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
16 DCPMMs and 24 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
24 DCPMMs and 24 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D

Table 27. Supported DCPMM capacity in App Direct Mode with four processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
8	16	L	√	√	√
		M	√	√	√
		Other	√	√	X
8	32	L	√	√	√
		M	√	√	√
		Other	√	√	
8	24	L	√	√	√
		M	√	√	√
		Other	√	√	
16	24	L	√	√	√
		M	√	√	
		Other	√		
24	24	L	√	√	√
		M	√	√	
		Other	√		

Table 28. Memory population in App Direct Mode with four processors (not interleaved only)

- **D: DRAM DIMMs with 16 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
1 DCPMM and 24 DIMMs	D		D		D		**P**	D		D		D	D		D		D			D		D		D
4 DCPMM and 24 DIMMs	D		D		D		**P**	D		D		D	D		D		D		**P**	D		D		D
Configuration	**Processor 3**												**Processor 4**											
	25	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**	**48**
1 DCPMM and 24 DIMMs	D		D		D			D		D		D	D		D		D			D		D		D
4 DCPMM and 24 DIMMs	D		D		D		**P**	D		D		D	D		D		D		**P**	D		D		D

Table 29. Supported DIMM capacity in App Direct Mode with four processors (not interleaved only)

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
1	24	L	√	√	√
		M	√	√	√
		Other	√	√	√
4	24	L	√	√	√
		M	√	√	√
		Other	√	√	

Memory Mode

In this mode, DCPMMs act as volatile system memory, while DRAM DIMMs act as cache.

Installation order: Memory Mode with two processors

Memory module installation order for DCPMM Memory Mode with two installed processors.

Table 30. Memory population in Memory Mode with two processors

- **D1: DRAM DIMMs of 16 or 32 GB**
- **D2: DRAM DIMMs of 32 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
4 DCPMMs and 8 DIMMs	**P**		D2		D2			D2		D2		**P**	**P**		D2		D2			D2		D2		**P**
4 DCPMMs and 12 DIMMs	D1		D1		D1	**P**	**P**	D1		D1		D1	D1		D1		D1	**P**	**P**	D1		D1		D1
8 DCPMMs and 12 DIMMs	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2
12 DCPMMs and 12 DIMMs	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2

Table 31. Supported DCPMM capacity in Memory Mode with two processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	8	L	√	√	√
		M	√	√	√
		Other	√	√	
4	12	L	√	√	√
		M	√	√	√
		Other	√	√	
8	12	L	√	√	√
		M	√	√	
		Other	√		√
12	12	L	√	√	√
		M	√	√	
		Other	√		√

Installation order: Memory Mode with four processors

Memory module installation order for DCPMM Memory Mode with four installed processors.

Table 32. Memory population in Memory Mode with four processors

- **D1: DRAM DIMMs of 16 or 32 GB**
- **D2: DRAM DIMMs of 32 GB or larger capacity**
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	Processor 3												Processor 4											
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
8 DCPMMs and 16 DIMMs	**P**		D2		D2			D2		D2		**P**	**P**		D2		D2			D2		D2		**P**
8 DCPMMs and 24 DIMMs	D1		D1		D1	**P**	**P**	D1		D1		D1	D1		D1		D1	**P**	**P**	D1		D1		D1
16 DCPMMs and 24 DIMMs	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2	D2		D2	**P**	D2	**P**	**P**	D2	**P**	D2		D2
24 DCPMMs and 24 DIMMs	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2	D2	**P**	D2	**P**	D2	**P**	**P**	D2	**P**	D2	**P**	D2

Table 33. Supported DCPMM capacity in Memory Mode with four processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
8	16	L	√	√	√
		M	√	√	√
		Other	√	√	
8	24	L	√	√	√
		M	√	√	√
		Other	√	√	
16	24	L	√	√	√
		M	√	√	
		Other	√		√
24	24	L	√	√	√
		M	√	√	
		Other	√		√

Mixed Memory Mode

In this mode, some percentage of DCPMM capacity is directly accessible to specific applications (App Direct), while the rest serves as system memory. The App Direct part of DCPMM is displayed as persistent memory, while the rest of DCPMM capacity is displayed as system memory. DRAM DIMMs act as cache in this mode.

Installation order: Mixed Memory Mode with two processors

Memory module installation order for DCPMM Mixed Memory mode with two installed processors.

Table 34. Memory population in Mixed Memory Mode with two processors

- **D: DRAM DIMMs of 16 GB or larger capacity**

  Note: 3DS LRDIMMs are not supported in this mode.
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
4 DCPMMs with 8 DIMMs	**P**		D		D			D		D		**P**	**P**		D		D			D		D		**P**
4 DCPMMs with 12 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
8 DCPMMs with 12 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
12 DCPMMs with 12 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D

Table 35. Supported DCPMM capacity in Mixed Memory Mode with two processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
4	8	L	√	√	√
		M	√	√	√
		Other	√	√	
4	12	L	√	√	√
		M	√	√	√
		Other	√	√	
8	12	L	√	√	√
		M	√	√	
		Other	√		√
12	12	L	√	√	√
		M	√	√	
		Other	√		√

Installation order: Mixed Memory Mode with four processors

Memory module installation order for DCPMM Mixed Memory mode with four installed processors.

Table 36. Memory population in Mixed Memory Mode with four processors

- **D: DRAM DIMMs of 16 GB or larger capacity**

  Note: 3DS LRDIMMs are not supported in this mode.
- **P: DC Persistent Memory Module (DCPMM)**

Configuration	Processor 1												Processor 2											
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	Processor 3												Processor 4											
	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
8 DCPMMs and 16 DIMMs	**P**		D		D			D		D		P	**P**		D		D			D		D		**P**
8 DCPMMs and 24 DIMMs	D		D		D	**P**	**P**	D		D		D	D		D		D	**P**	**P**	D		D		D
16 DCPMMs and 24 DIMMs	D		D	**P**	D	**P**	**P**	D	**P**	D		D	D		D	**P**	D	**P**	**P**	D	**P**	D		D
24 DCPMMs and 24 DIMMs	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D	D	**P**	D	**P**	D	**P**	**P**	D	**P**	D	**P**	D

Table 37. Supported DCPMM capacity in Mixed Memory Mode with two processors

Total PMMs	Total DIMMs	Processor Family	128 GB DCPMM	256 GB DCPMM	512 GB DCPMM
8	16	L	√	√	√
		M	√	√	√
		Other	√	√	
8	24	L	√	√	√
		M	√	√	√
		Other	√	√	
16	24	L	√	√	√
		M	√	√	
		Other	√		√
24	24	L	√	√	√
		M	√	√	
		Other	√		√

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